

IN THE CLAIMS:

1. (Previously Presented) A semiconductor device having a pixel matrix circuit that includes a pixel TFT and a storage capacitor:

wherein the pixel TFT has a channel formation region formed over a first wiring line with a first insulating layer interposed therebetween, and has a low concentration impurity region that is in contact with the channel formation region and overlaps the first wiring line;

wherein a gate electrode is formed over the channel formation region with a second insulating layer interposed therebetween;

wherein the gate electrode does not overlap the low concentration impurity region;

wherein the storage capacitor is formed:

from a capacitor wiring line,

from a semiconductor region that has the same composition as the channel formation region or the low concentration impurity region, and

from a part of the first insulating layer; and

wherein the first wiring line and the capacitor wiring line are formed on the same layer.

2. – 3. (Cancelled)

4. (Previously Presented) A semiconductor device according to claim 1,

wherein the first wiring line is appropriately a conductive film mainly containing an element selected from the group consisting of tantalum (Ta), chromium (Cr), titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si), or an alloy film or silicide film containing the above elements in combination, or a laminate of the conductive films, the alloy films, or the silicide films.

5. (Previously Presented) A semiconductor device according to claim 1,

wherein the channel formation region of the pixel TFT and the semiconductor region of the storage capacitor are formed of the same semiconductor layer.

6. (Previously Presented) A semiconductor device according to claim 1, wherein the first insulating layer is appropriately an oxide or halogenated compound containing an element selected from the group consisting of tantalum (Ta), titanium (Ti), barium (Ba), hafnium (Hf), bismuth (Bi), tungsten (W), thorium (Th), and lead (Pb).

7. (Previously Presented) A semiconductor device according to claim 1, wherein the first wiring line is in floating state.

8. (Previously Presented) A semiconductor device according to claim 1, wherein the first wiring line is kept at the lowest power supply electric potential.

9. (Previously Presented) A semiconductor device according to claim 1, wherein the pixel TFT is connected to the source wiring line and the gate wiring line, and the storage capacitor is formed under the source wiring line and/or the gate wiring line.

10. – 16. (Cancelled)

17. (Previously Presented) A semiconductor device, wherein the semiconductor device according to claim 1 is an active matrix liquid crystal display or an active matrix EL display.

18. (Previously Presented) A semiconductor device, wherein the semiconductor device according to claim 1 is a video camera, a digital camera, a projector, a projection TV, a goggle type display, an automobile navigation system, a personal computer, or a portable information terminal.

19. (Previously Presented) A semiconductor device according to claim 1, wherein a cross section of the first wiring line is taper shape.

20. (Previously Presented) A semiconductor device according to claim 1, wherein a cross section of the capacitor wiring line is taper shape.

21. (Cancelled).

22. (Previously Presented) The semiconductor device according to claim 1, wherein the insulating layer comprises a first insulating layer and a second insulating layer.

23-24. (Cancelled)

25. (Previously Presented) A semiconductor device according to claim 1, wherein the first wiring line and the gate electrode have the same electric potential.

26. (Previously Presented) A semiconductor device having a plurality of pixels which include a pixel TFT and a storage capacitor, wherein the pixel TFT has a channel formation region formed over a first wiring line with a first insulating layer and a second insulating layer interposed between the channel formation region and the first wiring line, and has a low concentration impurity region that is in contact with the channel formation region and overlaps the first wiring line;

wherein a gate electrode is formed over the channel formation region with a third insulating layer interposed therebetween;

wherein the gate electrode does not overlap the low concentration impurity region; wherein the storage capacitor is formed:

from a capacitor wiring line,

from a semiconductor region that has the same composition as the channel formation region or the low concentration impurity region, and

from the first insulating layer; and

wherein the first wiring line and the capacitor wiring line are formed on the same layer.

27. (Previously Presented) A semiconductor device having a plurality of pixels which include a pixel TFT and a storage capacitor,

wherein the pixel TFT has a channel formation region formed over a first wiring line with a first insulating layer, a second insulating layer, and a silicon oxide film interposed between the channel formation region and the first wiring line, and has a low concentration impurity region that is in contact with the channel formation region and overlaps the first wiring line;

wherein a gate electrode is formed over the channel formation region with a third insulating layer interposed therebetween;

wherein the gate electrode does not overlap the low concentration impurity region;

wherein the storage capacitor is formed:
from a capacitor wiring line,
from a semiconductor region that has the same composition as the
channel formation region or the low concentration impurity region, and
from a laminate of the first insulating layer and the silicon oxide film;
and
wherein the first wiring line and the capacitor wiring line are formed on the same
layer.

28. (Previously Presented) A semiconductor device according to claim 26,
wherein the first wiring line is appropriately a conductive film mainly containing an
element selected from the group consisting of tantalum (Ta), chromium (Cr), titanium (Ti),
tungsten (W), molybdenum (Mo), and silicon (Si), or an alloy film or silicide film containing
the above elements in combination, or a laminate of the conductive films, the alloy films, or
the silicide films.

29. (Previously Presented) A semiconductor device according to claim 26,
wherein the channel formation region of the pixel TFT and the semiconductor region
of the storage capacitor are formed of the same semiconductor layer.

30. (Previously Presented) A semiconductor device according to claim 26,
wherein the first insulating layer is appropriately an oxide or halogenated compound
containing an element selected from the group consisting of tantalum (Ta), titanium (Ti),
barium (Ba), hafnium (Hf), bismuth (Bi), tungsten (W), thorium (Th), and lead (Pb).

31. (Previously Presented) A semiconductor device according to claim 26,
wherein the first wiring line is in floating state.

32. (Previously Presented) A semiconductor device according to claim 26,
wherein the first wiring line is kept at the lowest power supply electric potential.

33. (Previously Presented) A semiconductor device according to claim 26,
wherein the pixel TFT is connected to the source wiring line and the gate wiring line,
and the storage capacitor is formed under the source wiring line and/or the gate wiring line.

34. (Previously Presented) A semiconductor device, wherein the semiconductor device according to claim 26 is an active matrix liquid crystal display or an active matrix EL display.

35. (Previously Presented) A semiconductor device according to claim 26, wherein the first wiring line and the gate electrode have the same electric potential.

36. (Previously Presented) A semiconductor device according to claim 27, wherein the first wiring line is appropriately a conductive film mainly containing an element selected from the group consisting of tantalum (Ta), chromium (Cr), titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si), or an alloy film or silicide film containing the above elements in combination, or a laminate of the conductive films, the alloy films, or the silicide films.

37. (Previously Presented) A semiconductor device according to claim 27, wherein the channel formation region of the pixel TFT and the semiconductor region of the storage capacitor are formed of the same semiconductor layer.

38. (Previously Presented) A semiconductor device according to claim 27, wherein the first insulating layer is appropriately an oxide or halogenated compound containing an element selected from the group consisting of tantalum (Ta), titanium (Ti), barium (Ba), hafnium (Hf), bismuth (Bi), tungsten (W), thorium (Th), and lead (Pb).

39. (Previously Presented) A semiconductor device according to claim 27, wherein the first wiring line is in floating state.

40. (Previously Presented) A semiconductor device according to claim 27, wherein the first wiring line is kept at the lowest power supply electric potential.

41. (Previously Presented) A semiconductor device according to claim 27, wherein the pixel TFT is connected to the source wiring line and the gate wiring line, and the storage capacitor is formed under the source wiring line and/or the gate wiring line.

42. (Previously Presented) A semiconductor device, wherein the semiconductor device according to claim 27 is an active matrix liquid crystal display or an active matrix EL display.

43. (Previously Presented) A semiconductor device according to claim 27, wherein the first wiring line and the gate electrode have the same electric potential.

44. (Previously Presented) A semiconductor device having a pixel matrix circuit and a driver circuit that are formed over the same substrate,
wherein a pixel TFT included in the pixel matrix circuit and an n-channel TFT included in the driver circuit each have a channel formation region formed over a first wiring line with an insulating layer interposed therebetween, and each have a low concentration impurity region that is in contact with the channel formation region and overlaps the first wiring line;
wherein a gate electrode is formed over the channel formation region with a second insulating layer interposed therebetween;
wherein the gate electrode does not overlap the low concentration impurity region;
wherein a storage capacitor included in the pixel matrix circuit is formed:
from a capacitor wiring line,
from a semiconductor region that has the same composition as the channel formation region or the low concentration impurity region, and
from a part of the insulating layer;
wherein the first wiring line and the capacitor wiring line are formed on the same layer; and
wherein the first wiring line connected to the pixel TFT has the lowest power supply electric potential, and the first wiring line connected to the n-channel TFT has at the same level of electric potential as the gate electrode.

45. (Previously Presented) A semiconductor device having a pixel matrix circuit and a driver circuit that are formed over the same substrate,
wherein a pixel TFT included in the pixel matrix circuit and an n-channel TFT included in the driver circuit each have a channel formation region formed over a first wiring line with a first insulating layer and a second insulating layer interposed between the channel formation region and the first wiring line, and each have a low concentration impurity region that is in contact with the channel formation region and overlaps the first wiring line;
wherein a gate electrode is formed over the channel formation region with a third insulating layer interposed therebetween;
wherein the gate electrode does not overlap the low concentration impurity region;
wherein a storage capacitor included in the pixel matrix circuit is formed:

from a capacitor wiring line,
from a semiconductor region that has the same composition as the
channel formation region or the low concentration impurity region, and
from the first insulating layer;
wherein the first wiring line and the capacitor wiring line are formed on the same
layer; and
wherein the first wiring line connected to the pixel TFT has the lowest power supply
electric potential, and the first wiring line connected to the n-channel TFT has the same level
of electric potential as the gate electrode.

46. (Previously Presented) A semiconductor device having a pixel matrix circuit
and a driver circuit that are formed over the same substrate,
wherein a pixel TFT included in the pixel matrix circuit and an n-channel TFT
included in the driver circuit each have a channel formation region formed over a first wiring
line with a first insulating layer, a second insulating layer, and a silicon oxide film interposed
between the channel formation region and the first wiring, and each have a low concentration
impurity region that is in contact with the channel formation region and overlaps the first
wiring line;
wherein a gate electrode is formed over the channel formation region with a third
insulating layer interposed therebetween;
wherein the gate electrode does not overlap the low concentration impurity region;
wherein a storage capacitor included in the pixel matrix circuit is formed:
from a capacitor wiring line,
from a semiconductor region that has the same composition as the
channel formation region or the low concentration impurity region, and
from a laminate of the first insulating layer and the silicon oxide film;
wherein the first wiring line and the capacitor wiring line are formed on the same
layer; and
wherein the first wiring line connected to the pixel TFT has the lowest power supply
electric potential, and the first wiring line connected to the n-channel TFT has the same level
of electric potential as the gate electrode.

47. (Previously Presented) A semiconductor device according to claim 44, wherein the first wiring line is appropriately a conductive film mainly containing an element selected from the group consisting of tantalum (Ta), chromium (Cr), titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si), or an alloy film or silicide film containing the above elements in combination, or a laminate of the conductive films, the alloy films, or the silicide films.

48. (Previously Presented) The semiconductor device according to claim 44, wherein the channel formation region of the pixel TFT and the semiconductor region of the storage capacitor are formed on the same semiconductor layer.

49. (Previously Presented) A semiconductor device according to claim 44, wherein the first insulating layer is appropriately an oxide or halogenated compound containing an element selected from the group consisting of tantalum (Ta), titanium (Ti), barium (Ba), hafnium (Hf), bismuth (Bi), tungsten (W), thorium (Th), thallium (Tl), and lead (Pb).

50. (Previously Presented) A semiconductor device according to claim 44, wherein the pixel TFT is connected to the source wiring line and the gate wiring line, and the storage capacitor is formed under the source wiring line and/or the gate wiring line.

51. (Previously Presented) A semiconductor device, wherein the semiconductor device according to claim 44 is an active matrix liquid crystal display or an active matrix EL display.

52. (Previously Presented) A semiconductor device according to claim 44, wherein the first wiring line is appropriately a conductive film mainly containing an element selected from the group consisting of tantalum (Ta), chromium (Cr), titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si), or an alloy film or silicide film containing the above elements in combination, or a laminate of the conductive films, the alloy films, or the silicide films.

53. (Previously Presented) The semiconductor device according to claim 44, wherein the channel formation region of the pixel TFT and the semiconductor region of the storage capacitor are formed on the same semiconductor layer.

54. (Previously Presented) A semiconductor device according to claim 45, wherein the first insulating layer is appropriately an oxide or halogenated compound containing an element selected from the group consisting of tantalum (Ta), titanium (Ti), barium (Ba), hafnium (Hf), bismuth (Bi), tungsten (W), thorium (Th), thallium (Tl), and lead (Pb).

55. (Previously Presented) A semiconductor device according to claim 45, wherein the pixel TFT is connected to the source wiring line and the gate wiring line, and the storage capacitor is formed under the source wiring line and/or the gate wiring line.

56. (Previously Presented) A semiconductor device, wherein the semiconductor device according to claim 45 is an active matrix liquid crystal display or an active matrix EL display.

57. (Previously Presented) A semiconductor device according to claim 46, wherein the first wiring line is appropriately a conductive film mainly containing an element selected from the group consisting of tantalum (Ta), chromium (Cr), titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si), or an alloy film or silicide film containing the above elements in combination, or a laminate of the conductive films, the alloy films, or the silicide films.

58. (Previously Presented) The semiconductor device according to claim 46, wherein the channel formation region of the pixel TFT and the semiconductor region of the storage capacitor are formed on the same semiconductor layer.

59. (Previously Presented) A semiconductor device according to claim 46, wherein the first insulating layer is appropriately an oxide or halogenated compound containing an element selected from the group consisting of tantalum (Ta), titanium (Ti), barium (Ba), hafnium (Hf), bismuth (Bi), tungsten (W), thorium (Th), thallium (Tl), and lead (Pb).

60. (Previously Presented) A semiconductor device according to claim 46, wherein the pixel TFT is connected to the source wiring line and the gate wiring line, and the storage capacitor is formed under the source wiring line and/or the gate wiring line.

61. (Previously Presented) A semiconductor device, wherein the semiconductor device according to claim 46 is an active matrix liquid crystal display or an active matrix EL display.